

16th International Test Synthesis Workshop

March 23-25, 2009
Austin, Texas, USA
<http://www.tttc-itsw.org>

Final Program

March 23, 2009 (Monday)

07:30 - 08:30 AM CONTINENTAL BREAKFAST

08:30 - 09:45 AM Opening Session

08:30 - 08:45 Opening Message Jennifer Dworak, General Chair

Keynote Address

08:45 - 09:45 *Test's Changing Role in the Late-Silicon Era* T. Cheng (UCSB)

09:45 - 10:45 AM Test Compression

Chair: B. Pouya (Freescale)

09:45 - 10:15 *Mask Sharing for Efficient X-Masking in Scan Compressed Designs* P. Dasgupta, B. Foutz, V. Kadam, S. Bhatia, S. Mukherjee, L. Basto* (Cadence)

10:15 - 10:45 *Efficient Linear Decompression Using ATE Vector Repeat-Per-All-Pins* J. Lee* (Intel), N. A. Touba (UT-Austin)

10:45 - 11:15 AM COFFEE BREAK

11:15 - 12:15 PM BIST

Chair: E. Macdonald (UT-El Paso)

11:15 - 11:45 *Clock Monitoring Simulations for BIST Verification* S. Hwang, I. Kim, A. Guettaf (Broadcom)

11:45 - 12:15 *Optimized Distributed Simulation of Logic BIST Patterns* J. Udell, G. Mrugalski, T. Rinderknecht* (Mentor)

12:15 - 01:30 PM LUNCH

01:30 - 03:00 PM Delay Test

Chair: K. Balakrishnan (AMD)

01:30 - 02:00 *An Evaluation of Frequency vs Switching Activity Using At-speed Structural Patterns* T. McLaurin*, C. Hawkins (ARM)

02:00 - 02:30 *Evaluation of Speed Path Identification of Structural Tests* J. Zeng, H.-C. Yu, M. Mateja*, J. Wang (AMD), Li-C. Wang (UCSB)

02:30 - 03:00 *Unsensitizable Path Identification at RTL Using High-Level Synthesis Information* S. Ohtake*, N. Ikeda, M. Inoue, H. Fujiwara (NAIST, Japan)

03:00 - 03:30 PM COFFEE BREAK

03:30 - 05:00 PM Functional Test and Debug

Chair: J. Wingfield (AMD)

03:30 - 04:00 *Considering Functional Behavior for Probabilistic Defect Detection* C. Ashley-Rollman, Y. Shi, J. Dworak* (Brown Univ.)

04:00 - 04:30 *Selecting Signals to Observe for Silicon Debug* J.-S. Yang**, N. A. Touba (UT-Austin)

04:30 - 05:00 *Test and Debug Tools for High Lane-Count, High Speed I/O in a Production Environment* P. Cadorette*, J. Turek (TI)

05:00 - 06:30 PM Fault Tolerance and Reliability

Chair: P. Joshi (Intel)

05:00 - 05:30 *A Fault-Tolerant Technique for Analog Filters* S. Askari, A. Namazi, M. Nourani* (UT-Dallas)

05:30 - 06:00 *Improving Memory ECC by Exploiting Unused Spare Columns* R. Datta**, N. A. Touba (UT-Austin)

06:00 - 06:30 *3D Simulation and Analysis of the Radiation Tolerance of Voltage Scaled Digital Circuits* R. Garg**, S. P. Khatri (Texas A&M)

DINNER (On Your Own)

* Presenter, ** Student Presenter

March 24, 2009 (Tuesday)

07:00 - 08:00 AM CONTINENTAL BREAKFAST

08:00 - 09:00 AM Keynote Address

Getting More Out of Test: Addressing Variability and DFM

Anne Gattiker (IBM)

09:00 - 10:00 AM DFT

09:00 - 09:30

Improving Memory Repair by Selective Row Partitioning

Chair: M. Nourani (UT-Dallas)

T. Rab**, A. Bawa, N. A. Touba (UT-Austin)

09:30 - 10:00

A Robust Pulse-triggered Flip-flop and an Enhanced Scan Cell Design

T. Soni, R. Kumar**, S. P. Khatri (Texas A&M)

10:00 - 10:30 AM COFFEE BREAK

10:30 - 11:30 AM Industry Standards and Practices

10:30 - 11:00

Towards a Comprehensive Scan-Based Delay Test Methodology

Chair: M. Reese (AMD)

S. Patil (Intel)

11:00 - 11:30

P1687 2009 Update: The Story of IJTAG

A. Crouch (ASSET InterTech)

11:30 - 03:00 PM LUNCH AND SOCIAL EVENT (CRUISE ON TOWN LAKE)

03:00 - 04:00 PM Embedded Tutorial I

The Whys and Whats of an IEEE 1500 Wrapper

Chair: J. Doege (AMD)

T. McLaurin (ARM)

04:00 - 04:15 PM COFFEE BREAK

04:15 - 06:15 PM PANEL: Move Over Time Zero Test, On-line is Here to Stay

Moderator: P. Joshi (Intel)

Panelists: S. Patil (Intel)

T. Cheng (UCSB)

T. Munns (Consultant, TAMU)

T. Skergan (IBM)

A. Nahar (TI)

DINNER (On Your Own)

March 25, 2009 (Wednesday)

07:00 - 08:00 AM CONTINENTAL BREAKFAST

08:00 - 09:30 AM ATPG and Fault Simulation

08:00 - 08:30

Low Cost Test Generation for Delay Test

Chair: M. Mateja (AMD)

Z. Wang**, D. M. H. Walker (Texas A&M)

08:30 - 09:00

Fault Table Generation Using Graphics Processing Units

K. Gulati**, S. P. Khatri (Texas A&M)

09:00 - 09:30

Enhancement Approaches for Constant Test Power Algorithm

Z. Jiang**, D. M. H. Walker (Texas A&M)

09:30 - 10:30 AM Embedded Tutorial II

Coming Soon to an SoC or SiP Near You – The IEEE 1149.7

Chair: J. Zeng (AMD)

Reduced-Pin and Enhanced-Functionality Test Access Port

A. Ley (ASSET InterTech)

10:30 - 11:00 PM COFFEE BREAK

11:00 - 12:00 PM DFT

11:00 - 11:30

Column-Addressable Multiple Scan Architecture for Low Power Testing and Delay Testing

Chair: R. Putman (Cirrus)

S. P. Lin, C. L. Lee* (NCTU, Taiwan), J.-J. Chen, K.-L. Luo, W. C. Wu (ITRI, Taiwan)

11:30 - 12:00

Low Cost Design-for-Testability Features of an Industrial Control Application SoC

C. ZhiKuang, H. Kai (Southeast Univ., China)

12:00 - 12:15 PM ITSW 2009 Best Student Paper Award

12:15 PM ADJOURN