

15th International Test Synthesis Workshop

April 7-9, 2008
Santa Barbara, California, USA
<http://www.tttc-itsw.org>

Final Program

April 7, 2008 (Monday)

7:30 - 8:15 AM CONTINENTAL BREAKFAST

8:15 - 9:15 AM Opening Session

8:15 – 8:30 Opening Message Nilanjan Mukherjee, General Chair

Keynote Address

8:30 – 9:15 *DFT Needs Charms to Soothe the Savage (Test Data) Beast* Ken Butler (TI)

9:15 - 10:15 AM Test Optimization

Chair: X. Lin (Mentor Graphics)

9:15 – 9:45 *A Methodology for Functional Black-Box Testing of Non-Processor Cores in an SOC* S. Gurumurthy, S. Sambamurthy, J. Abraham (UT-Austin)

9:45 – 10:15 *Efficient Production Test Selection and Ordering based on Functional Fault Grading* J.H. Jeong, D. Mahon, M. Laisne (Qualcomm), A. Ambler (UT-Austin)

10:15 - 10:45 AM COFFEE BREAK

10:45-12:15 PM DFT

Chair: C. Dixit (LSI)

10:45 - 11:15 *Strategies for Power-Aware DFT* V. Chickermane, P. Gallagher, K. Chakravadhanula (Cadence)

11:15 - 11:45 *Clock Gating to Improve At-Speed Scan* D. Dehnert (Intel)

11:45 - 12:15 *Update: the P1687 (IJAG) Hardware Proposal for Efficient Embedded Instrument Access, Bandwidth, and Connectivity* A. Crouch (Asset-Intertech), J. Rearick, K. Posse (AMD)

12:15 – 1:30 PM LUNCH

1:30 - 3:30 PM Test Generation and Diagnosis

Chair: A. Crouch (Asset-Intertech)

1:30 - 2:00 *On Tests to Detect Interconnect Opens in Digital CMOS Circuits* S. Reddy (U. Iowa), I. Pomeranz (Purdue), C. Liu, and J. Howard (U. Iowa)

2:00 - 2:30 *Test Generation for Interconnect Opens* X. Lin, J. Rajski (Mentor Graphics)

2:30 - 3:00 *Using Design Validation Input Sequences to Determine Fault Criticality for Test Set Optimization* Y. Shi, K. DiPalma, W.-C. Hu, J. Dworak (Brown)

3:00 - 3:30 *Diagnosis of Design Related Issues with Feature Encoding and Ranking* P. Bastani, N. Callegari, L. Wang (UCSB)

3:30 - 4:00 PM COFFEE BREAK

4:00 – 6:00 PM Test Using Wireless Communication

Chair: C.-W. Wu (NTHU)

4:00 - 4:30 *Wireless Testing of RAM Chips by HOY: Methodology, Architecture, and Prototype Implementation* T.-Y. Chang, C.-T. Huang, J.-J. Liou, C.-W. Wu, H.-P. Ma, C.-C. Tien, C.-H. Wang, C.-U. Yang

4:30 - 5:00 *Wireless Communications Interface Design for HOY Wireless Testing Scheme* M.-Y. Chu, T.-Y. Chang, H.-J. Hsu, C.-Y. Lee, C.-F. Li, H.-P. Ma, C.-T. Huang, P.-C. Huang

5:00 - 5:30 *Improving the Efficiency of Scan Test on Wireless HOY Test Platform* C.-W. Tzeng, C.-Y. Lin, S.-Y. Huang, C.-T. Huang, J.-J. Liou, H.-P. Ma, C.-W. Wu

5:30 - 6:00 *Automatic Wrapper Synthesis and Test Program Generation for Packet-based ATE Platforms* Y.-Y. Chen, C.-U. Yang, S.-Y. Chen, J.-J. Liou

DINNER (On Your Own)

April 8, 2008 (Tuesday)**7:30 - 8:30 AM CONTINENTAL BREAKFAST****8:30 - 10:30 AM Scan and BIST****Chair: H. Walker (Texas A&M)**

- 8:30 - 9:00 *Scan-Chain Design and Optimization for Three-Dimensional Integrated Circuits*
X. Wu, P. Falkenstern (Penn State), K. Chakrabarty (Duke), and Y. Xie (Penn State)
- 9:00 - 9:30 *Using an X-Canceling MISR with Deterministic Observation for Increasing Output Compaction in Presence of Unknowns*
R. Putman, R. Garg, and N.A. Touba (UT-Austin)
- 9:30 - 10:00 *LBIST: a Myth or a Reality*
S. Hwang, A. Guettaf, S. Ganta (Broadcom)

10:00-10:30 AM COFFEE BREAK**10:30–12:00PM Delay Test****Chair: T.M. Mak (Intel)**

- 10:30 – 11:00 *Scalable Identification of High Quality Path Delay Tests Under Launch-Off-Capture Scan Architecture*
E. Flanigan, M. Goparaju, D. Jayaraman, S. Tragoudas (S. Illinois), M. Laisne, H. Cui, T. Petrov (Qualcomm)
- 11:00 – 11:30 *An Efficient Dynamic Compaction Approach for Path Delay Test*
Z. Wang, D.M.H. Walker (Texas A&M)
- 11:30 – 12:00 *A Path-Oriented Timing-Aware Diagnosis Methodology of At-Speed Structural Tests*
J. Wang, J. Zeng, M. Mateja (AMD)

12:00 - 1:30 PM LUNCH**1:30 - 3:30 PM Fault Detection****Chair: R. Daasch (Portland State)**

- 1:30 – 2:00 *On Detecting Scan Chain Internal Faults*
F. Yang (U. Iowa), S. Chakravarty, N. Devta-Prasanna (LSI), S.M. Reddy (U. Iowa), I. Pomeranz (Purdue)
- 2:00 – 2:30 *A Modified Scan-D Flip-Flop Design to Reduce Test Power*
S. Khatri, S. Ganesan (Texas A&M)
- 2:30 – 3:00 *Time-Multiplexed Online Checking: A Feasibility Study*
M. Gao, H.-M. Chang, P. Lisherness, K.-T. Cheng (UCSB)
- 3:00 – 3:30 *A Fault-Tolerant Mechanism for Analog Systems*
A. Namazi, S. Askari, M. Nourani (UT-Dallas)

3:30 - 4:00 PM COFFEE BREAK**4:00 - 6:00 PM PANEL: Fast Clocks, Low Power, and Small Geometries: Big Problems for Test?****Moderator: Saghir Shaikh (Cadence)**

- Panelists:** Tsvetomir Petrov (QualComm)
T.M. Mak (Intel)
Al Crouch (ASSET InterTech)
Hank Walker (Texas A&M)
Rohit Kapur (Synopsys)

6:30 – 9:30 PM SOCIAL EVENT AND DINNER**April 9, 2008 (Wednesday)****7:30 - 8:30 AM CONTINENTAL BREAKFAST****8:30 - 10:00 AM Test and Fault Tolerance****Chair: M. Nourani (UT-Dallas)**

- 8:30 – 9:00 *Expanding Observation Window for Trace Buffer via Selective Data Capture*
J.-S. Yang, N. Touba (UT-Austin)
- 9:00 - 9:30 *Study on Test Power Reduction for Scan-Based Hybrid BIST*
M. Arai, A. Suto, K. Iwasaki (Tokyo Met. Univ.)
- 9:30 – 10:00 *Design of a Fault Tolerant Carry Lookahead Adder*
C.-Y. Huang, T.-H. Ko, J.-L. Huang (NTU)

10:00-10:30 AM COFFEE BREAK**10:30-12:00 PM Test Generation and Reliability****Chair: S. Khatri (Texas A&M)**

- 10:30 – 11:00 *Test Generation for Designs with Multiple Clocks*
X. Lin (Mentor), S. Reddy (U. Iowa)
- 11:00 – 11:30 *Reliable Nanometer VLSI Systems using NMR Logic Gates*
A. Namazi, M. Nourani (UT-Dallas)
- 11:30 – 12:00 *Reducing the Cost of Test – An Adaptive Test Solution*
R. Turakhia, M. Ward (LSI), R. Daasch (Portland State)

12:00 PM ADJOURN