

14th International Test Synthesis Workshop

March 5-7, 2007
El Tropicana Riverwalk Hotel, San Antonio, Texas, USA
<http://www.tttc-itsw.org>

Final Program

March 5, 2007 (Monday)

8:00 - 9:00 AM PLATED BREAKFAST: MEETING ROOM FOYER

9:00 – 10:00AM Opening Session

9:00 –9:15 Opening Message Srinivas Patil, General Chair
9:15 – 10:00 **Keynote Address** Jacob Abraham, University of Texas at Austin
The Future of Test: Evolution or Revolution?

10:00-10:30 AM COFFEE BREAK

10:30 AM-Noon DFT

10:30 – 11:00 *DFT vs. DFD* Chair: Jason Doege (DA-Test)
Nikhil Dakwala (Stridge, Inc.)
11:00 – 11:30 *DFT Diversity for Systematic Defects* Irith Pomeranz, Sudhakar M. Reddy, and Srikanth Venkataraman (Purdue, U of Iowa, Intel)
11:30 – 12:00 *A System for Automatic Insertion of IEEE 1500 Compliant Wrappers* Krishna Chakravadhanula and Vivek Chickermame (Cadence)

Noon–1:30 PM LUNCH

1:30– 2:30 PM Debug and Diagnosis

1:30 – 2:00 *Accurately Determining Bridging Defects from Layout* Chair: TM Mak (Intel)
Maria Gkatziani, Rohit Kapur, Su Qing, Ben Mathew, Roberto Mattiuzzo, Laura Tarantini, Cy Hay, Salvatore Talluto and T. W. Williams (Synopsys, STMicroelectronics, U. Calgary)
2:00 – 2:30 *Fast Failing Chip Diagnosis using a Small Dictionary* Wei Zou, Wu-Tung Cheng, Sudhakar M. Reddy, Huaxing Tang (Mentor and U. of Iowa)

2:30 – 4:00 PM Delay Test

2:30 – 3:00 *Using Boolean Satisfiability to Eliminate False Aggressor Combinations in Timing Analysis* Chair: James Wingfield (AMD)
Abhijit Jas, Kip Killpack, Chandramouli Kashyap, Debasish Das, Hai Zhou (Intel, Northwestern)
* 3:00- - 3:30 *Statistical Learning for Test Optimization: Making Decisions Beyond Pass and Fail* Sean Wu, Benjamin N. Lee, Janine C-Y Chen, Li-C Wang (UCSB)
3:30 – 4:00 *On Common-Mode Skewed-Load and Broadside Tests* Irith Pomeranz, Sudhakar M. Reddy (Purdue, U of Iowa)

4:00 – 4:30 PM COFFEE BREAK

4:30 – 6:00 PM Built In Self Test and Self Repair

4:30 – 5:00 *Turn-Key BIST* Chair: Hank Walker (Texas A&M)
Bahram Pouya (Freescale)
* 5:00 – 5:30 *RTL Coding Considerations for Digital to Analogue Converter BIST Core Generation* Jeffrey Ryan, I. Grout, and T. O'Shea (U. of Limerick)
5:30 – 6:00 *A Low Impact, Programmable Memory BIRA System* Steve Gregor (Cadence)

DINNER (On Your Own)

March 6, 2007 (Tuesday)

7:30 – 8:30 AM CONTINENTAL BREAKFAST: MEETING ROOM FOYER

8:30–10:00PM	Tools for Enhanced Test Generation and Analysis	Chair: Sunil Khatri (Texas A&M)
8:30 – 9:00	<i>Logic Simulation on Graphics Processors</i>	Atchuthan S. Perinkulam, Sandip Kundu (U. of Massachusetts, Amherst)
9:00 – 9:30	<i>Boolean Satisfiability Algorithms in Hardware</i>	Abhijit Jas, Srinivas Patil, Kanupriya Gulati (Intel, Texas A&M)
* 9:30 – 10:00	<i>An Extended Critical Path Tracing Approach for Combinational Circuits</i>	Lei Wu, D. M. H. Walker (Texas A&M)

10:00-10:30 AM COFFEE BREAK

10:30–12:30 AM	Test Compression I	Chair: Luis Basto (Cadence)
10:30 - 11:00	<i>Reducing Stuck-at Fault Pattern Counts through Low-Power Segmented Scan</i>	Zhuo Zhang, Sudhakar M. Reddy, Irith Pomeranz, Bashir Al-Hashimi (U of Iowa, Purdue, U of Southampton)
11:00 - 11:30	<i>A Seed-Selection Method to Increase Defect Coverage for LFSR Reseeding-Based Test Compression</i>	Zhanglei Wang, Krishnendu Chakrabarty, Michael Bienek (Duke Univ., AMD)
11:30 – 12:00	<i>Improving Test Compression Using Multiple Expansion Ratios and Dependency Analysis</i>	Richard Putman and Nur Touba (Cirrus Logic, UT Austin)
12:00 – 12:30	<i>How to Compact Output Responses with X's Using a MISR without Losing Fault Coverage via Symbolic Simulation</i>	Nur Touba (UT Austin)

12:30 – 1:00 PM BREAK

1:00 – 3:30 PM LUNCH and SOCIAL EVENT: Riverwalk Cruise

3:30 - 5:00 PM	PANEL: <i>The Top of Testing's Most Wanted List: What is the most critical testing challenge? (or have all the bad guys been caught already?)</i>	Moderator: Carl Barnhart (SiliconAid)
	Jason Doege (DA-Test)	
	T. M. Mak (Intel)	
	Rob Dassch (Portland State University)	
	Sunil Khatri (Texas A&M University)	
	Tom Williams (Synopsys)	
	Luis Basto (Cadence)	

DINNER (On Your Own)

March 7, 2006 (Wednesday)

7:30 - 8:30 AM CONTINENTAL BREAKFAST: MEETING ROOM FOYER

8:30 – 10:30 AM	Online Testing and Fault Tolerance	Chair: Nur Touba (UT Austin)
8:30 - 9:00	<i>Online Testing of Asynchronous Handshake circuits by Protocol Decomposition</i>	Deepali Koppad (Univ. of Edinburgh)
* 9:00 - 9:30	<i>A Robust Interconnect Mechanism for Nanometer VLSI</i>	A. Namazi, M. Nourani and M. Saquib (UT Dallas)
* 9:30 – 10:00	<i>Using Fault Tolerant Methods in DFT Circuitry</i>	L. David Armbrust and W. Robert Daasch (Portland State University)

10:00 – 10:20 AM COFFEE BREAK

10:20 – 11:50 PM	Test Compression II	Chair: Nilanjan Mukherjee (Mentor)
10:20 – 10:50	<i>Improved Scan Chain Failure Diagnosis Resolution with Compressed Patterns</i>	Ruifeng Guo, Yu Huang, Wu-Tung Cheng (Mentor)
10:50 – 11:20	<i>On the need to overcome challenges in Achieving Target Compression</i>	Saket K. Goyal, Thai Nguyen, Arun Gunda (LSI Logic)
11:20 – 11:50	<i>Test Point Insertion at RTL to Reduce Transition Test Volume</i>	Kedarnath J. Balakrishnan (AMD)

11:50 – 12:00 PM CLOSING REMARKS AND ADJOURN